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09/353,120	07/14/1999	LOUIS F. VILLAROSA JR.	061607-1100	3012

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EXAMINER
KUMAR, PANKAJ

ART UNIT	PAPER NUMBER
2631	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/353,120	Applicant(s) VILLAROSA ET AL.	
	Examiner Pankaj Kumar	Art Unit 2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-4, 6-8, 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by McMahan et al. U.S. Patent no. 5,870,446.

3. Regarding claim 1, McMahan et al. shows in figure 1, a circuit for detecting errors in the synchronization of a DTE data signal (11) with a DCE clocking signal (43 and 55) in a communication environment wherein the DCE interfaces the DTE to a communication channel at an interface rate determined by the DCE clocking signal (43 and 55), the circuit comprising:

a. a master clock producing a master clock signal (HS CLK) having a frequency greater than the frequency of the DCE clocking signal. At the end of the first full paragraph of column 6, it is implied that the master clock signal is 16 MHz and the DCE clocking signal is 1.544 MHz;

b. a clock generator (55) deriving a circuit clocking signal from said master clock signal (HS CLK input to 48), said circuit clocking signal having the same frequency as the DCE clocking signal;

c. a sample enable generator (15) for generating a first sample enable signal at a first time and a second sample enable signal at a second time; and

d. a sample comparator (21) for using said first sample enable signal and said second enable signal to obtain a first sample of said DTE data signal (11) at said first time and a second sample of said DTE data signal at said second time, and for determining whether the DTE data signal (11) has undergone a transition (21) during the time interval between said first time and said second time.

4. Regarding claim 2, figure 1 in McMahan et al. shows the circuit of claim 1 wherein the frequency of said master clock signal is approximately 8 times the frequency of said DCE clocking signal. At the end of the first full paragraph of page 6, it is implied that the master clock signal is 16 MHz and the DCE clocking signal is 1.544 MHz.

5. Regarding claim 3, figure 1 in McMahan et al. shows the circuit of claim 1 wherein the time interval between said first time and said second time is approximately 1/8 of the period of said DCE clocking signal. The data sampling shift register (15) is sampling at 16 MHz which is approximately 1/8 of the period of the 1.544 MHz DCE clocking signal.

6. Regarding claim 4, figure 1 in McMahan et al. shows the circuit of claim 1 wherein said sample comparator (21) generates a selector control signal (23) if said first sample is said first sample is different from said second sample.

7. Regarding claim 6, McMahan et al. shows in figure 1, a circuit for detecting errors in the synchronization of a DTE data signal (11) with a DCE clocking signal (43 and 55) in a communication environment wherein the DCE interfaces the DTE to a communication channel, the circuit comprising:

e. means for obtaining a first sample of said DTE data signal at a first time (15)

f. means for obtaining a second sample of said DTE data signal at a second time (15), said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal. The interval between the first and second time is 1/(16 MHz), which is less than 1/(1.544MHz), the period of the DCE clocking signal.

g. means for comparing said first sample to said second sample (21)

8. Regarding claim 7, figure 1 in McMahan et al. shows the circuit of claim 6 wherein the interval between said first time and said second time is approximately 1/8 of the period of the DCE clocking signal. The data sampling shift register (15) is sampling at 16 MHz which is approximately 1/8 of the period of the 1.544 MHz DCE clocking signal.

9. Regarding claim 8, figure 1 in McMahan et al. shows the circuit of claim 6 further comprising means for generating a selector control signal (23) if said first sample is different from said second sample.

10. Regarding claim 11, McMahan et al. shows in figure 1, a method for detecting errors in the synchronization of a DTE data signal (11) with a DCE clocking signal (43 and 55) in a communication environment wherein the DCE interfaces the DTE to a communication channel, the method comprising the steps of:

h. obtaining a first sample of said DTE data signal at a first time (15)

i. obtaining a second sample of said DTE data signal at a second time (15), said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal. The interval between the first and second time is 1/(16 MHz), which is less than 1/(1.544MHz), the period of the DCE clocking signal.

j. comparing said first sample to said second sample (21)

11. Regarding claim 12, figure 1 in McMahan et al. shows the method of claim 11 wherein the interval between said first time and said second time is approximately 1/8 of the period of the DCE clocking signal. The data sampling shift register (15) is sampling at 16 MHz which is approximately 1/8 of the period of the 1.544 MHz DCE clocking signal.

12. Regarding claim 13, figure 1 in McMahan et al. shows the method of claim 11 further comprising the step of generating a selector control signal (23) if said first sample is different from said second sample.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over McMahan et al. as applied to claim 4 above, and further in view of Hata U.S. Patent no. 5,479,455.

15. The McMahan reference shows the circuit of claim 4 as described above. McMahan does not show an inverter producing an inverted circuit clocking signal from said circuit clocking signal; and a selector producing an output signal that is selected from the group consisting of said circuit clocking signal and said inverted circuit clocking signal, in response to said selector control signal. Hata in figure 8 shows an inverter (17) producing an inverted circuit clocking signal (b) from said circuit clocking signal (a); and a selector (20–21) producing an output signal that is selected from the group consisting of said circuit clocking signal and said inverted circuit clocking signal, in response to said selector control signal (h). McMahan may be modified in view of Hata by putting Hata's figure 8 output (g) as the input in McMahan at 43 in figure 1. McMahan's 23 in figure 1 can serve as the selector control signal or enable (h) for Hata's figure 8. It would have been obvious at the time of the invention to one having skill in the art to combine McMahan et al. with Hata for the benefit of a more synchronous clocking circuit. If data is latched at the rising edge of a clock and if the clock is inverted, the time of the rising edge will be different between the clock and the inverted clock. Thus the latching of the data will be delayed. This will foster synchronization. Hata realizes that there exists a time delay between

the transmitter and the receiver by stating in the first paragraph of column 10, that the occurrence of the noise is different from the receiving unit and the transmitting unit. Hata also states in the first full paragraph of column 7 that the transition has to occur for a predetermined period of time by saying: "In the transmit unit of the clock synchronous serial information transfer apparatus of the first invention, when the clock level transition has occurred, the signal is propagated between the first and second signal holding circuits holding the information signal to be transmitted for transmission, only when the level transition has continued over a predetermined time, and the influence of noise is eliminated." Since the transition has to occur for a period of time, Hata is essentially causing a delay in latching the data to minimize the influence of a delayed transceiver operation.

16. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over McMahan et al. as applied to claim 8 above, and further in view of Hata. The McMahan reference shows the means of claim 8 as described above. McMahan does not show a means for inverting said DCE circuit clocking signal in response to said selector control signal. Hata, in figure 8, shows a means for inverting said DCE circuit clocking signal (b) in response to said selector control signal (h). McMahan may be modified in view of Hata by putting Hata's figure 8 output (g) as the input in McMahan at 43 in figure 1. McMahan's 23 in figure 1 can serve as the selector control signal or enable (h) for Hata's figure 8. It would have been obvious at the time of the invention to one having skill in the art to combine McMahan et al. with Hata for the benefit of a more synchronous clocking circuit as discussed above.

17. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over McMahan and Hata. The McMahan reference along with the Hata reference show the means for claim 9 as

described above. What the McMahan reference does not show is a means for transmitting said inverted DCE clocking signal from said DCE to said DTE in lieu of said DCE clocking signal. Hata, in figure 8, shows a means for transmitting said inverted DCE clocking signal (b) from said DCE (2 in figure 1) to said DTE (1 in figure 1) in lieu of said DCE clocking signal (a). McMahan may be modified in view of Hata by replacing McMahan's TX Clock Generator (55) output (TX Clock) with Hata's figure 8 output (g). Hata's figure 8 output (g) can then serve as the input to a DTE. It would have been obvious at the time of the invention to one having skill in the art to combine McMahan et al. with Hata for the benefit of a more synchronous communication between a DCE and a DTE as discussed above.

18. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over McMahan et al. as applied to claim 13 above, and further in view of Hata. The McMahan reference shows the means of claim 13 as described above. McMahan does not show the step of inverting said DCE circuit clocking signal in response to said selector control signal. Hata, in figure 8, shows a step for inverting said DCE circuit clocking signal (b) in response to said selector control signal (h). McMahan may be modified in view of Hata by putting Hata's figure 8 output (g) as the input in McMahan at 43 in figure 1. McMahan's 23 in figure 1 can serve as the selector control signal or enable (h) for Hata's figure 8. It would have been obvious at the time of the invention to one having skill in the art to combine McMahan et al. with Hata for the benefit of a more synchronous clocking method.

19. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over McMahan and Hata. The McMahan reference along with the Hata reference show the means for claim 9 as described above. What the McMahan reference does not show is the step of transmitting said

inverted DCE clocking signal from said DCE to said DTE in lieu of said DCE clocking signal. Hata, in figure 8, shows the step of transmitting said inverted DCE clocking signal (b) from said DCE (2 in figure 1) to said DTE (1 in figure 1) in lieu of said DCE clocking signal (a). McMahan may be modified in view of Hata by replacing McMahan's TX Clock Generator (55) output (TX Clock) with Hata's figure 8 output (g). Hata's figure 8 output (g) can then serve as the input to a DTE. It would have been obvious at the time of the invention to one having skill in the art to combine McMahan et al. with Hata for the benefit of a more synchronous communication between a DCE and a DTE.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (703) 305-0194. The examiner can normally be reached on 8:30 AM to 5:30 PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on (703) 305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

PK
January 2, 2002

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 1/3/02